A Magnetic Digital Storage System

By ANDREW D. BOOTH, Ph.D.*

DESCRIPTIONS have appeared[1,2] of storage devices for use in serial operation calculating machines, but in this country at least, little emphasis has been placed on the other possible type of computing system, namely, that employing parallel operation. It is not proposed to give any discussion of computing machines in this paper but for completeness it must be stated that in serial operation machines the digits of a number become available, and are used, one at a time starting usually from the least significant, whereas in a parallel operation machine all the digits of any number become available at the same time.

Without wishing to become controversial, it may be remarked that von Neumann, who was the originator of many of the current ideas on calculating machines, has abandoned the serial operation machine in favour of its parallel operation counterpart.

Requirements for a Storage Device

In either type of calculating machine the requirements of the storage device are similar, and are as follows:

(1) The storage should be permanent if desired.

(2) The contents of any position must be erasible at will and capable of replacement by new data.

(3) The volumetric efficiency should be high.

(4) The access and replacement time of stored data should be small.

The delay line storage device of Wilkes[1] and the cathode-ray tube memory of Williams[2] satisfy all of the above requirements except (1) and to a less extent (3). Either of these devices loses all its stored data if a power supply failure occurs. In addition, in the forms described by the authors, neither is directly suitable for a parallel operation machine.

The idea of using the well known principles of magnetic sound recording for the storage of digital data seems to have occurred to a number of designers at about the same time, the system to be described in this paper, however, is thought to be the first in actual operation.

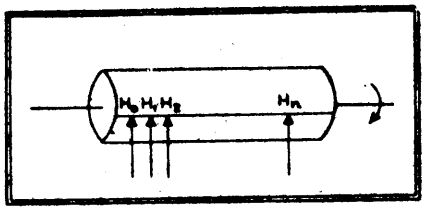
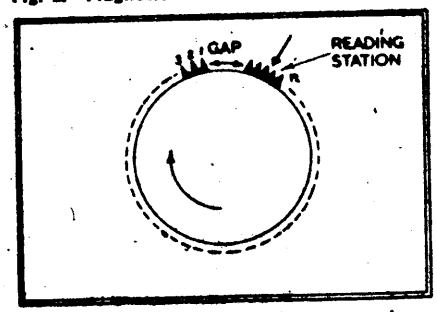


Fig. 1. Magnetic drum and read/record heads

Fig. 2. Magnetic state of clock pulse track



Principles of the Magnetic Memory

Essentially, the storage device consists of a cylindrical drum coated with permanent magnetic material and rotating under a series of read/record heads arranged along a generator of the cylinder. In Fig. 1 H_1-H_n are a set of these heads.

All of the digits of any particular number, which is in binary form (*e.g.*, Wilkes[1]), are recorded and read off simultaneously by the heads.

Successive numbers are recorded in sequence as the drum rotates and to distinguish between them an extra track (H_0) is added which contains a set of equispaced positive "clock" pulses.

In order to determine the position of the first number it is necessary to indicate the start of this clock pulse track. This could be done in various ways; for example, it might start with a single negative pulse, or alternatively a separate track might contain a single pulse to indicate the zero position of the clock pulse track. In fact, it turns out to be much simpler to leave a small gap, clear of any pulses, at the end of the clock pulse track, and to use this as a zero indication. The general appearance of the magnetic state of the clock pulse track is then shown in Fig. 2.

In order to go to any position on the drum and to read or record there, all that is necessary is to count from the zero position on the clock track and to arrange that the counter emits a pulse when it reaches the given position. A schematic diagram of the whole memory is given in Fig. 3.

The positive pulse input from the clock track head is amplified and sent to the binary counter C, which is arranged to zero on receipt of a pulse from the shaping circuit contained in A_0.

The contents of C are compared with the required memory location as shown by a set of position number inputs; when the two numbers

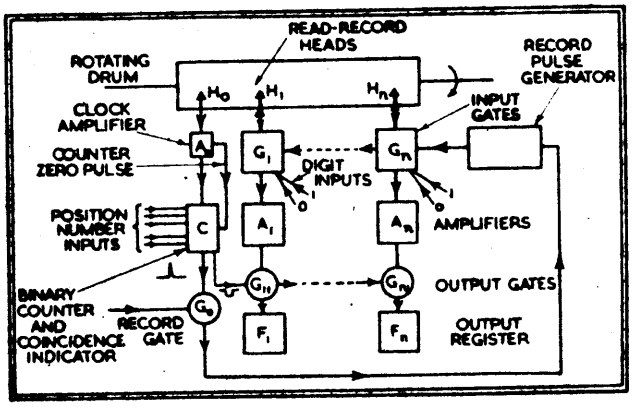


Fig. 3. Schematic of magnetic storage

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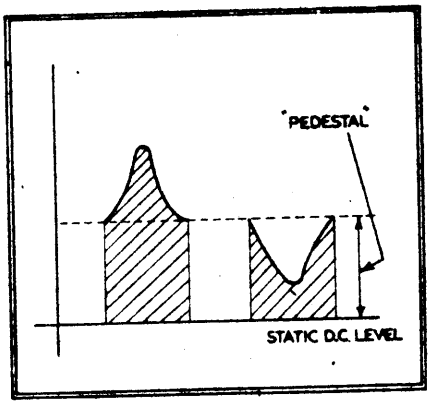


Fig. 16. Output from common gate circuits

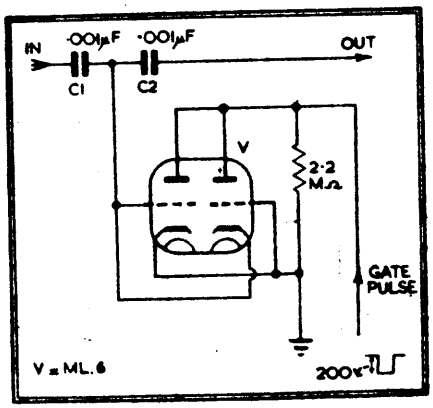


Fig. 17. Gate circuit

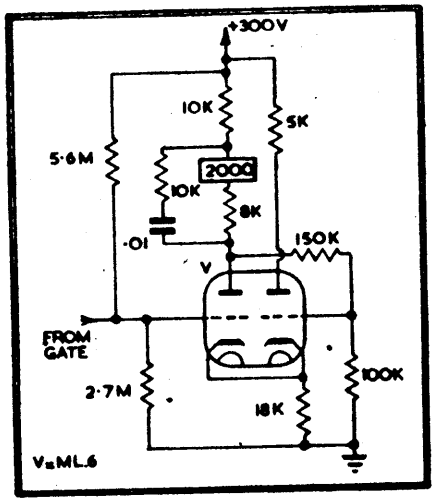


Fig. 18. Toggle output circuit

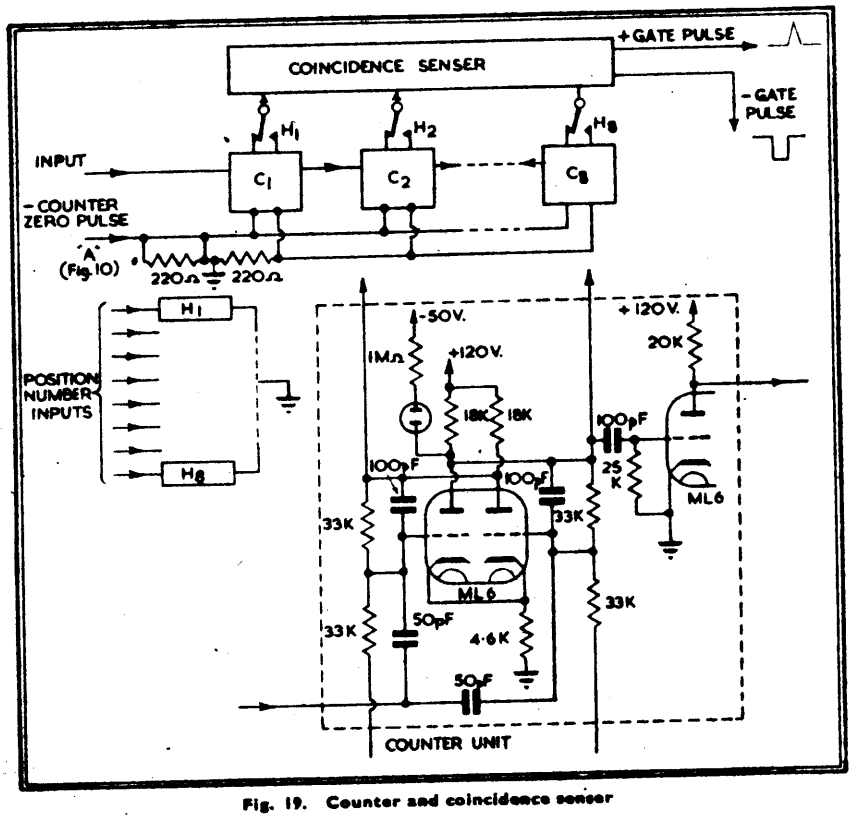


Fig. 19. Counter and coincidence sensor

possible to generate a gate signal which extends over one-half of the output pulse only, and thus to select a positive or negative pulse corresponding to unity or zero. Most of the published gate circuits have the disadvantage of placing the output on a "pedestal" as shown in Fig. 16, or else of transmitting pulses of one sign only.

To remedy this defect the circuit of Fig. 17 was devised.

In the absence of a gate pulse the twin triode grids act as diodes and short-circuit incoming signals of either sign to earth. On applying a large negative pulse to the two anodes the electrons are repelled to the cathodes and the resistance of the grid circuits rises sharply. If, in this condition, a voltage variation occurs on C_1 it is transmitted via C_2 to the flip-flop; in the absence of the gate pulse, however, nothing passes.

The Output Stage.

This consists of the standard cathode-coupled toggle, shown in Fig. 18.

For reliable operation it was necessary to compensate the inductance of the relay coil, and the network shown behaves like a pure resistance.

Conclusion

It will be seen from the above circuit descriptions and from the photograph of Fig. 8 that the storage system described in this paper is considerably more compact than any hitherto disclosed. Although in its present form it is somewhat slow in operation it is quite easy to speed up the rotation of the cylinder and to record and read data at several stations around the drum. In this way availability times of better than 1 millisecond could be realised. Work is at present proceeding along these lines and it appears that the necessary modifications are trivial in nature.

The author wishes to express his sincere thanks to Dr. Geoffrey Gee, Director of Research, and to the Board of the British Rubber Producers' Research Association for supporting this work, and also to Miss X. Sweeting and Dr. R. W. Williams for assistance in construction.

References

1 Wilkes and Renwick ELECTRONIC ENGINEERING 20, 208, (1948).
2 Williams and Kilburn, *Journal I.E.E.* (In press.)

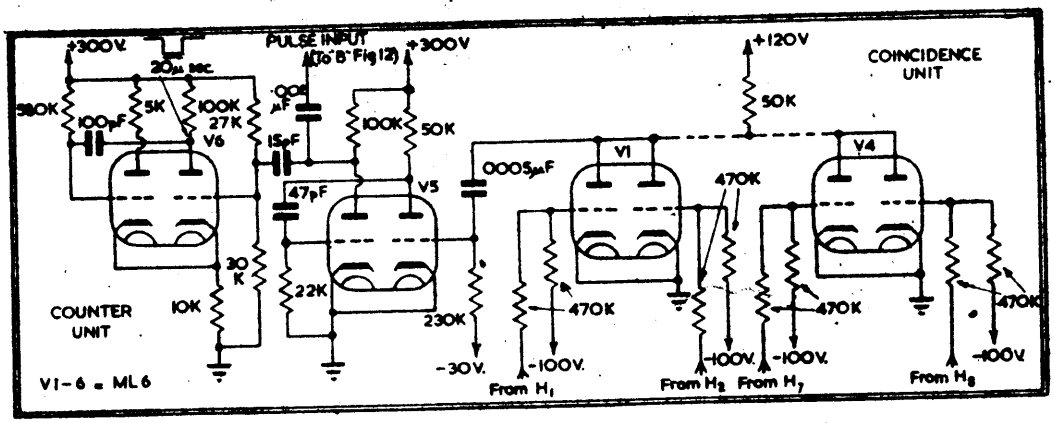


Fig. 11. Counter and coincidence unit

tents and relay do not agree, however, the coincidence valve conducts. Since the resistance of any coincidence valve is only about 7 KΩ, if at least one valve is conducting the potential at the common anode load cannot rise above 7/57 × 120 = 15 volts, which is well below the cut-off of the first stage of V_5. The second stage of V_5 acts as an inverter and pulse shaper, since a sharp positive trigger pulse is required for the input pulse generator.

V_5 generates a negative pulse of 220 volts amplitude and 15 μsec. duration which is used to gate the outputs from the digit amplifiers into their respective flip-flops.

The Input Pulse Generator.

Since the heads have an input impedance of less than 0.1 Ω and require pulse currents of 10-20 amps., a special generator had to be designed. Thyratron circuits were tried, but were found to be unreliable and liable to parasitic oscillation. Eventually the circuit shown in Fig. 12 was devised and gives completely satisfactory results.

In the present memory the record gate G_6 is a relay, but it would be simple to substitute an electronic element. In the absence of a gating pulse via G_6 the blocking oscillator is held off by the bias. The transformer produces a pulse of less than 1 μsec. duration and the cathode follower transformer enables the whole head array to be pulsed.

The Input Gates.

These are constructed from relay elements and are shown in Fig. 13.

Each gate element consists of two relays having two change-over contacts which are activated from the main circuits of the machine. When relay "1" is operated the head is pulsed in the positive sense, and when relay "0" is operated in the negative sense.

The gate action isolates the digit track amplifiers during pulsing, as the stray pulse which crosses the relay contacts due to capacitative coupling does not effect the input transformers, which have extremely low input impedance.

The Digit Amplifiers.

These are perfectly straightforward R-C coupled amplifiers, again constructed to give low gain below 10 Kc/s. A typical circuit is shown in Fig. 14.

The Output Gate.

It is desired to gate the amplifier output into a flip-flop circuit at a given position only, the two possible amplifier output pulse shapes being shown in Fig. 15.

Since the clock pulse occurs at the origin in the above sketches, it is

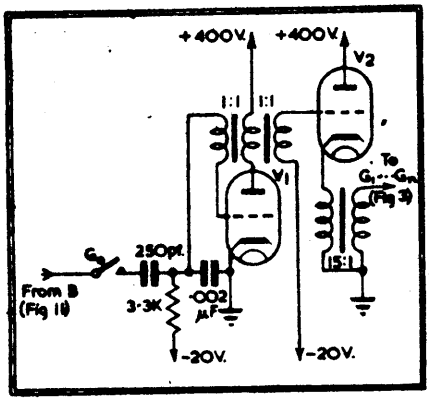


Fig. 12. Input pulse generator

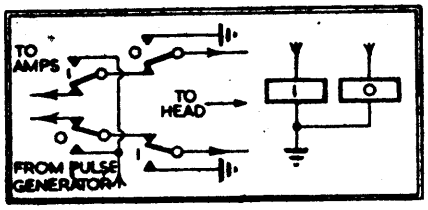


Fig. 13. Relay input gate

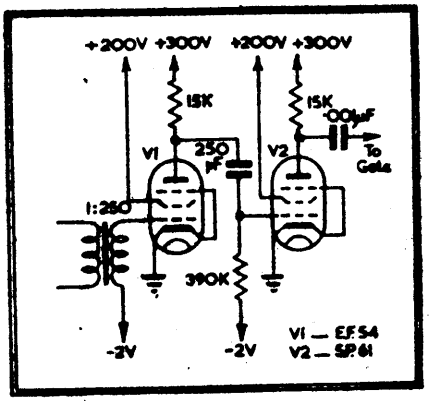


Fig. 14. Typical digit amplifier

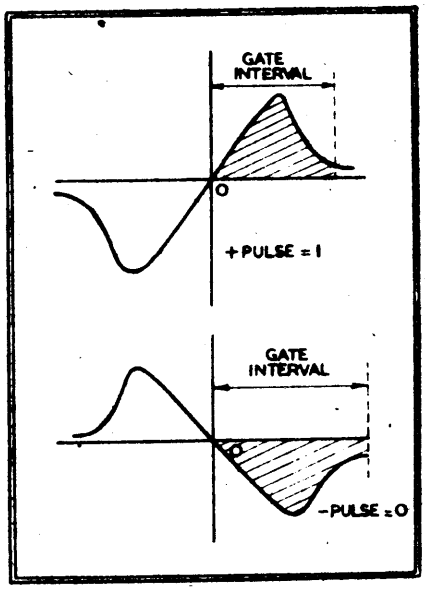


Fig. 15. Output waveforms for "1" and "0"

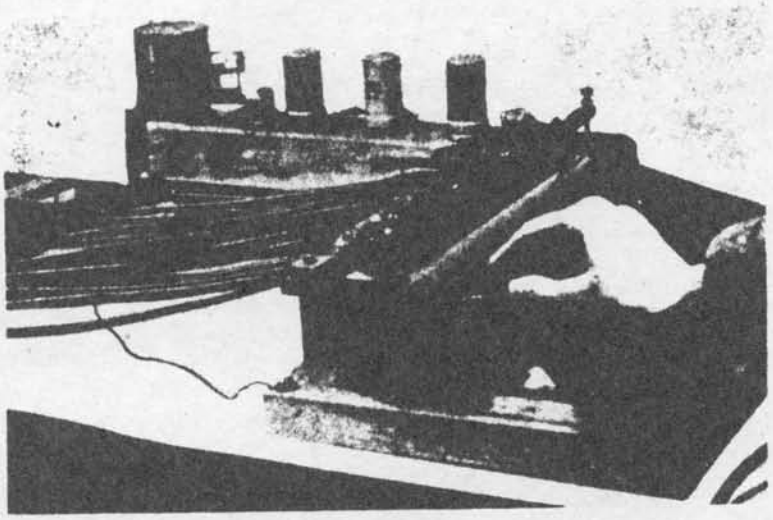


Fig. 8. Model of drum with heads mounted in position

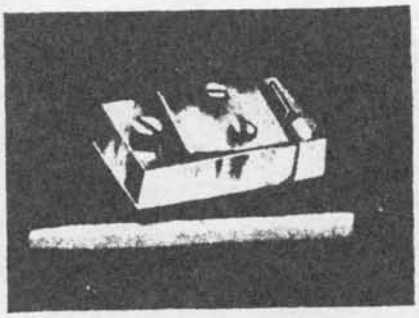


Fig. 9. One of the final read/record heads

Mechanical Construction

A photograph of the cylinder and head assembly is given in Fig. 8.

For mathematical reasons it was decided to have 21 binary digit numbers and to store 256 such quantities. With the packing of 50 digits/in. and surface speed of 25 ft./sec., this resulted in a cylinder 2 in. in diameter and 12 in. long rotating at 3,000 r.p.m. The maximum waiting time for reading or recording is 20 m.sec. and the mean time 10 m.sec.

The heads, shown in detail in Fig. 9, are mounted on a brass bar and are individually adjustable by means of a simple screw assembly. Coarse adjustment is provided for aligning the main bar and the drum surface.

Circuits

At the outset it can be stated that all relays are of the Siemens high speed variety with 1000 + 1000Ω coils. The measured time of closure or operation of these is less than 2 m.sec. Relays are drawn in the normal position.

The Clock Track Amplifier.

On this track it is necessary to reproduce with accuracy the sharp transition between the two turning points in output voltage shown in Fig. 6, and it was decided that a bandwidth of at least 200 Kc/s. was needed. The amplifier circuit of Fig. 10 proved adequate.

It will be noticed that the grid coupling and screen resistor by-pass time constants are so chosen that there is a steep reduction in gain below 10 Kc/s. This makes the amplifier very much more stable and makes inter-stage decoupling unnecessary. In particular, 50 c/s. pick-up and microphonic noise from V_1 are imperceptible. V_1 is biased below cut-off to enable the noise background from the medium to be clipped off. This is necessary, since the gap at the end of the clock pulse track (Fig. 2) may contain a noise pulse of sufficient amplitude to trigger the counter after it has been set to zero.

The output of V_1 is fed directly to the input of the binary counter and a portion is rectified by the IN34 germanium diode and applied as a negative potential to the grid leak of the blocking oscillator tube V_4. This keeps the latter from firing until the clock pulse track gap is reached, when the charge on C leaks away via R. The firing of V_4 sends a pulse via the output winding of T to the grid load resistor of the counter, thus "zero-ing" the latter.

The Counter and Coincidence Senser.

The counter used is an ordinary scale-of-two circuit with buffer amplifier to remove unwanted pulses.' The circuit constants are chosen so that the counter is reliable up to 100 Kc/s.

Counter Unit

It will be seen from Fig. 11 that when any one of the counter stages C_n is in the same state ("0" or "1") as its associated relay H_n, the potential of the grid of the corresponding coincidence valve falls below cut off. When counter con-

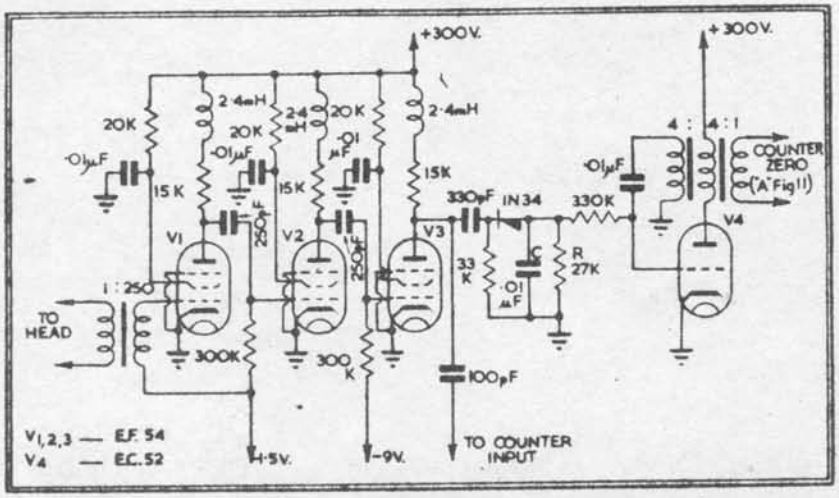


Fig. 10. Clock pulse amplifier, shaper and counter zero generator

agree a pulse is emitted by a circuit. Normally this pulse opens a set of gates G_{11}-G_{n1}, which allow the output pulses from the digit track heads H_1-H_n to set a series of flip-flop storage elements F_1-F_n to the digit pattern recorded under the heads in the given position. When it is desired to record in a given position a gate G_0 allows the above coincidence pulse to trigger a "record pulse" generator which sends either positive ("1") or negative ("0") pulses, via the input gates G_1-G_n, to the heads. It should be noted that prior to the record operation the input gate will have been set to "0" or "1" positions from digit input leads, and that the nature of the storage is such that the input data automatically erases that already present.

In the present memory, intended for use with A.R.C. (Automatic Relay Computer), the input gates G_1-G_n, the record gate G_0 and part of the counter-coincidence circuit are relay elements, and the output flip-flops set relays to operate the remainder of the machine.

The Magnetic Circuit

While many highly specialised magnetic recording media exist, these are at present difficult to obtain in suitable form, and it was decided to use a thin plating of electrolytic nickel. Although the magnetic properties of this seem to leave much to be desired, the medium is quite good enough for the purpose in hand. In the final design a plated layer between .0005 in. and .001 in. in thickness was used. Extensive experiments showed that up to 100 digits/in. could be recorded, but for safety it was decided to use only a 50 digits/in. packing

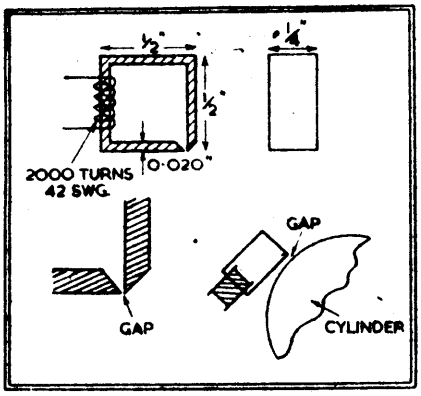


Fig. 4. Early recording head

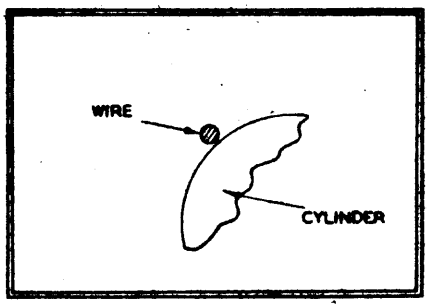
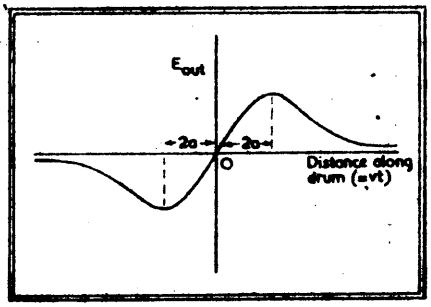


Fig. 5. Single wire head

Fig. 6. Output voltage from single wire head



as this allowed for considerable variations in head construction. The surface speed of the drum was 25 ft./sec.

The first models of the recording heads were of the form shown in Fig. 4.

Single laminations of .020 in. silicon iron were used and the heads were run in contact with the cylinder as shown. Using 2,000 turns on the magnetising coils it was found that the shortest recording pulse which could be used was 35 μsec. This left much to be desired and further experiments were instituted.

About this time Dr. Julian Bigelow* suggested using a single, very fine wire as recording head.

This was to be mounted in close proximity to the drum surface and pulsed with a current of between 10 and 50 amps. Since the current flows for considerably less than 1 μsec. this does not damage the wire. It can be shown that if the input pulse is short enough for the recording medium not to move appeciably during the pulse, the output voltage follows the law:

$$E_{out} = K\, v^2 i t / (4a^2 + v^2 t^2)$$

where

v = surface speed of medium
i = recording current
a = distance of wire centre from drum surface
t = time.

The general form of this function is shown in Fig. 6.

In the present memory, with digit packing of 50/in., it follows that for non-interference of pulses $4a << .020$ in. or $a << .005$ in.; this means that wires of diameter less than .002 in. must be used. Handling becomes difficult with .001 in. diameter wire and problems arise in the design of step-up transformers for ratio of 1:100 and bandwidths of 250 Kc/s. where the input impedance is about 1Ω.

As a comparison, tests were made using a .002 in. diameter single wire and a single lamination head of the general type shown in Fig. 4, but reduced to one-half the linear dimensions. With ten turns this gave precisely the same output as the single wire, thus indicating losses of about 90 per cent.

It had been evident that the performance improved as the linear dimensions of the heads decreased and a series of experiments were tried with very small heads. These resulted in the design shown in Fig. 7.

Using a single 32-gauge wire as magnetising source, the output signal was three times greater than that from a .001 in. diameter wire, indicating that the loss in efficiency is no longer important. With the same design it proved possible to insert four turns of 42-gauge wire through the window and 12 times the single wire head output was obtained. The output pulse shape is identical with that of Fig. 6.

In order to record "1" and "0" on the medium the simple procedure of pulsing the head with sufficient current to cause magnetic saturation of the nickel was adopted. Thus, if "1" is recorded with a pulse of +20 amps., to record "0" a −20 amp. pulse is superimposed.

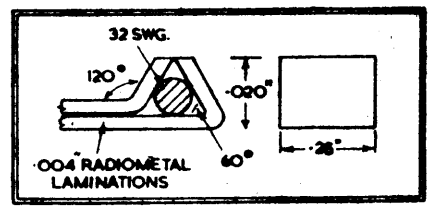


Fig. 7. Final head design

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